CLAIMS

What is claimed is:

1. A computer system comprising a microprocessor having a dynamically re-configurable trace cache to provide application specific configuration of the trace cache.

2. The computer system of claim 1 wherein the trace cache comprises:

a tag array;

a data array; and

a next fetch address (NFA) array.

3. The computer system of claim 2 wherein the tag array, the data array and NFA array each store one or more fetch address entries and one or more temporal address entries.

4. The computer system of claim 3 wherein each trace stored in the trace cache is assigned an index value.

5. The computer system of claim 4 wherein the tag array, the data array and the NFA array each comprise a decoder to access a trace stored in the one or more temporal address entries using an index value.

6. The computer system of claim 3 wherein the one or more temporal address entries are generated by simulating to identify dynamic traces, the

execution behavior of the dynamic traces and generating an index value for each identified trace.

7. A method comprising:

generating an index value to be associated with a first instruction trace;

storing the first trace within a first of a plurality of cache array entries using an index value associate with the first trace; and

retrieving the first trace from the first cache array entry using the index value associated with the first trace.

8. The method of claim 7 further comprising storing a second instruction trace within the plurality of cache array entries using a fetch address if there is no index value associated with the second trace.

9. The method of claim 8 further comprising retrieving the second trace from the plurality of cache array entries using the fetch address.

10. The method of claim 7 further comprising:

simulating a trace cache to identify the execution behavior of the first trace; and

attaching the index number to a branch instruction that forms the first trace.

11. The method of claim 7 wherein generating an index value comprises:

collecting profile information on traces that are to be generated; and

generate indexes for each of the traces.

12. The method of claim 11 wherein collecting profile information comprises:

recording a fetch address and path number for each of a plurality of fetched traces; and

identifying traces that are frequently executed.

13. The method of claim 12 further comprising generating a temporal relationship graph for the frequently executed traces, the temporal relationship graph indicating a temporal relationship between two or more of the frequently executed traces.

14. The method of claim 13 further comprising allocating each of the frequently executed traces to the plurality of cache array entries, wherein traces having temporal relationships are allocated to different cache array entries.

15. The method of claim 13 further assigning an index value for each frequently executed trace after generating the temporal relationship graph.

16. A microprocessor comprising:

an instruction cache to receive and store the micro-operations as cache lines;

a trace cache, coupled to the instruction cache, that is dynamically re-

configurable using profile information to provide application specific configuration of the trace cache; and

an execution core to execute the micro-operations.

17. The microprocessor of claim 16 further comprising:

a fill unit to form micro-operations; and

branch prediction logic.

18. The microprocessor of claim 16 wherein the trace cache comprises:

a tag array;

a data array; and

a next fetch address (NFA) array.

19. The microprocessor of claim 18 wherein the tag array, the data array and NFA array each store one or more fetch address entries and one or more temporal address entries.

20. The microprocessor of claim 19 wherein each trace stored in the trace cache is assigned an index value.

21. The microprocessor of claim 20 wherein the tag array, the data array and the NFA array each comprise a decoder to access a trace stored in the one or more temporal address entries using an index value.

22. A trace cache comprising:

a tag array;

a data array; and

a next fetch address (NFA) array;

wherein the tag array, the data array and NFA array each store one or more fetch address entries and one or more temporal address entries.

23. The microprocessor of claim 22 wherein each trace stored in the trace cache is assigned an index value.

24. The microprocessor of claim 23 wherein the tag array, the data array and the NFA array each comprise a decoder to access a trace stored in the one or more temporal address entries using an index value.

25. The microprocessor of claim 22 wherein the one or more temporal address entries are generated by simulating to identify dynamic traces, the execution behavior of the dynamic traces and generating an index value for each identified trace.

26. A computer system comprising:

a microprocessor having a dynamically re-configurable trace cache to provide application specific configuration of the trace cache;

a chipset coupled to microprocessor; and

a main memory coupled to the chipset.

provide application specific configuration of the trace cache;

a chipset coupled to microprocessor; and

a main memory coupled to the chipset.

27. The computer system of claim 26 wherein the trace cache comprises:

a tag array;

a data array; and

a next fetch address (NFA) array.

28. The computer system of claim 27 wherein the tag array, the data array and NFA array each store one or more fetch address entries and one or more temporal address entries.

29. The computer system of claim 28 wherein each trace stored in the trace cache is assigned an index value.

30. The computer system of claim 29 wherein the tag array, the data array and the NFA array each comprise a decoder to access a trace stored in the one or more temporal address entries using an index value.